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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,623	12/22/2000	Richard A. Keeney	MGI-174	4584

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EXAMINER	
SHAPIRO, LEONID	
ART UNIT	**PAPER NUMBER**
2673	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/748,623	KEENEY ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *2,3,7-10,14,16,17,21-24 and 28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,11-13,15,18-20,25-27 and 29-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 11-13, 15, 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurogane (US Patent No. 6,259.424 B1) in view of Krusius et al. (US Patent No. 6,005,649) and Lambert (US Patent No. 6,816,143 B1) and Yamazaki et al. (US Patent No. 6,147,667).

As to claim 1, Kurogane teaches a method for mitigating defects caused by inoperative pixels in liquid crystal display built on a silicon integrated circuit substrate (See Col. 5, Lines 3-34), substrate having an integral metal-oxide semiconductor (MOS) control chip (See Col. 8, Lines 11-15) containing MOS drive circuitry (See Fig. 1, items 1A, 1B, 10, Col. 6, Lines 41-45, from Col. 1, Line 65 to Col. 7, Line 2), comprising: identifying defective MOS drive circuitry for the inoperative pixel (See Fig. 4, items 21A, 22, Col. 8, Lines 16-38) after fabrication of MOS control chip (See Col. 8, Lines 11-15); disconnecting the defective drive circuitry from inoperative pixel (See Fig.7, items 1A, 33, Col. 9, Lines 51-57).

Kurogane does not show connecting the inoperative pixel to a working drive circuit of nearby pixel, the detective drive circuitry is by passed and inoperative pixel is

driven from working drive circuit of a nearby circuit, nearby pixel comprising one of adjacent or a non-adjacent pixel.

Lambert teaches connecting the inoperative column of pixels to a working drive circuit of nearby column of pixels, the detective drive circuitry is by passed and inoperative pixel column is driven from working drive circuit of a nearby circuit nearby pixel column comprising one of adjacent or a non-adjacent pixel column (See Fig. 3, items 43, 45, Col. 96, Lines 3-7).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Lambert into the Kurogane system in order to be capable of self-diagnostic and repair (See Col. 1, Lines 6-10).

Kurogane and Lambert do not show micro-display and CMOS control chip and CMOS drive circuitry.

Krusius et al. teaches the back plane of a typical micro-display is formed from a crystalline silicon chip includes CMOS integrated circuits (See Col. 2, Lines 1-4) and CMOS driver circuit (See Col. 2, Lines 27-30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use micro-display and CMOS integrated circuits using typical SRAM process as shown by Krusius et al. in the Kurogane and Lambert system for repairing MOS panels in order to reduce size of display to 10X7 mm (See Col. 1, Lines 31-35).

Krusius et al., Kurogane and Lambert do not show using a bypass bit latch, such that when a bypass bit is set, the defective drive circuitry is bypassed.

Yamazaki et al. teaches the latch circuit controlled the bit signals (See Fig. 12B and 12C, items 63-71, in description See Col. 24, Lines 1-7).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use bit latch as bypass latch as shown by Yamazaki et al. in the Krusius et al., Kurogane and Lambert apparatus and method in order to repair panels having sufficiently few defects.

As to claim 15, Kurogane teaches mitigating defects caused by inoperative pixels in liquid crystal display, comprising:

a plurality of pixels (See Fig. 17, item 2, Col. 2, Lines 1-13);

an integral metal-oxide semiconductor (MOS) control chip (See Col. 8, Lines 11-15) containing MOS drive circuitry (See Fig. 1, items 1A, 1B, 10, Col. 6, Lines 41-45, from Col. 1, Line 65 to Col. 7, Line 2), comprising: identifying defective MOS drive circuitry for the inoperative pixel (See Fig. 4, items 21A, 22, Col. 8, Lines 16-38) after fabrication of MOS control chip (See Col. 8, Lines 11-15);

means for disconnecting the defective drive circuitry from inoperative pixel (See Fig.7, items 1A, 33, Col. 9, Lines 51-57).

Kurogane does not show connecting the inoperative pixel to a working drive circuit of nearby pixel, the detective drive circuitry is by passed and inoperative pixel is driven from working drive circuit of a nearby circuit, nearby pixel comprising one of adjacent or a non-adjacent pixel.

Lambert teaches connecting the inoperative column of pixels to a working drive circuit of nearby column of pixels, the detective drive circuitry is by passed and

inoperative pixel column is driven from working drive circuit of a nearby circuit nearby pixel column comprising one of adjacent or a non-adjacent pixel column (See Fig. 3, items 43, 45, Col. 96, Lines 3-7).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Lambert into the Kurogane system in order to be capable of self-diagnostic and repair (See Col. 1, Lines 6-10).

Kurogane and Lambert do not show micro-display and CMOS control chip and CMOS drive circuitry.

Krusius et al. teaches the back plane of a typical micro-display is formed from a crystalline silicon chip includes CMOS integrated circuits (See Col. 2, Lines 1-4) and CMOS driver circuit (See Col. 2, Lines 27-30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use micro-display and CMOS integrated circuits using typical SRAM process as shown by Krusius et al. in the Kurogane and Lambert system for repairing MOS panels in order to reduce size of display to 10X7 mm (See Col. 1, Lines 31-35).

Krusius et al., Kurogane and Lambert do not show using a bypass bit latch, such that when a bypass bit is set, the defective drive circuitry is bypassed.

Yamazaki et al. teaches the latch circuit controlled the bit signals (See Fig. 12B and 12C, items 63-71, in description See Col. 24, Lines 1-7).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use bit latch as bypass latch as shown by Yamazaki et al. in the Krusius et

al., Kurogane and Lambert apparatus and method in order to repair panels having sufficiently few defects.

As to claims 11, 25, Kurogane teaches pixels repaired in groups (See Fig. 10A, 10B, items yi and yi+1, in description See Col. 10, Lines 52-58).

As to claims 12, 26, Kurogane teaches identifying defective drive circuitry comprises the further step of providing test circuitry associated with the display (See Fig. 4, items 21A, 22, Col. 8, Lines 16-38).

As to claims 13, 27, Kurogane teaches pixel drive circuitry associated with each pixel is located separately from each pixel (See Fig. 4, items 1A,3A,1B,3B, in description See Col. 7, Lines 1-33).

2. Claims 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., the Krusius et al., Kurogane and Lambert as applied to claim 1 above, and further in view of Hiroki (US Patent No. 6, 618, 115 B1).

Yamazaki et al., the Krusius et al., Kurogane and Lambert do not show defective CMOS drive circuitry is identified after the CMOS control chip and the liquid crystal material assembled together via optical inspection of the display after assembly of display.

Hiroki teaches defective CMOS drive circuitry is identified after the CMOS control chip and the liquid crystal material assembled together via optical inspection of the display after assembly of display (See Figs 5-6, items 301-307, in description See Col. 6, Lines 16-28 and 51-67, Col. 10, Lines 4-8).

It would have been obvious to one of ordinary skill in the art at the time of the invention to identify defective CMOS drive circuitry after the CMOS control chip and the liquid crystal material assembled together via optical inspection of the display after assembly of display as shown by Hiroki in Yamazaki et al., the Krusius et al., Kurogane and Lambert apparatus and method in order to repair panels having sufficiently few defects.

3. Claims 4, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., the Krusius et al., Kurogane and Lambert as aforementioned in claims 1 and 15 in view of Yamazaki et al. (US Patent No. 6, 147, 667).

Yamazaki et al., the Krusius et al., Kurogane and Lambert do not show additional circuitry with a bypass bit latch, such when bypass bit latch is set from an external memory, the detective drive circuitry is bypassed and the inoperative pixel is driven from the working drive circuit of the nearby pixel.

Yamazaki et al. teaches the latch circuit controlled the bit signals (See Fig. 12B and 12C, items 63-71, in description See Col. 24, Lines 1-7).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use bit latch as shown by Yamazaki et al. in the Yamazaki et al., the Krusius et al., Kurogane and Lambert apparatus and method in order to repair panels having sufficiently few defects.

4. Claims 5, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., the Krusius et al., Kurogane and Lambert as aforementioned in claims 1 and 15 in view of Yang (US Patent No. 6,392,427 B1).

Yamazaki et al., the Krusius et al., Kurogane and Lambert do not show multiplexing the drive circuits of each pixel with the drive circuit of a nearby pixel.

Yang teaches multiplexer and drive array to route test patterns (See Fig 4, items 400, 406, 408, in description see Col. 4, lines 55-59).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use multiplexer as shown by Yang in the Yamazaki et al., the Krusius et al., Kurogane and Lambert apparatus and method in order to repair panels having sufficiently few defects.

5. Claims 6, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., the Krusius et al., Kurogane and Lambert as aforementioned in claims 1 and 15 in view of Anholm et al. (US Patent No. 5,043,655).

Yamazaki et al., the Krusius et al., Kurogane and Lambert do not show tri-state transistor associated with each pixel connected to the bypass latch and resistor coupling neighboring pixels, such that when the bypass bit is set, the transistor is switched to bypass the detective drive circuitry so that the inoperative pixel is driven from the working drive circuit of a nearby pixel through resistor.

Kurogane teaches to connect nearby pixel (See Fig. 7, items 2A,2B,33).

Anholm et al. teaches tri-state control (See Fig. 4, items 50-56, in description see Col. 7, Lines 29-45).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a tri-state transistor with bypass latch and resistor as shown by Anholm et al. in the Yamazaki et al., the Krusius et al., Kurogane and Lambert. apparatus and method in order to repair panels having sufficiently few defects.

Response to Amendment

6. Applicant's arguments filed on 10/13/05 with respect to claims 1, 4-6, 11-13, 15, 18-20, 25-27, 29-32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

The Katoh et al. (US Patent No. 5,926,156) reference discloses matrix type image display using backup circuitry.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ls 03.17.05

VIJAY SHANKAR
PRIMARY EXAMINER